This listing of claims will replace all prior versions and listings of claims in the application:

1.   (Currently Amended) A multiply-accumulate module comprising:

a multiply-accumulate core, wherein said multiply-accumulate core comprises:

a plurality of Booth encoder cells;

a plurality of Booth decoder cells connected to at least one of said Booth encoder cells~~, said plurality of Booth decoder cells including at least one first Booth decoder cell and at least one second Booth decoder cell, said at least one first Booth decoder cell structurally the same as said at least one second Booth decoder cells~~; and

a plurality of Wallace tree cells connected to at least one of said Booth decoder cells~~, said plurality of Wallace tree cells including at least one first Wallace tree cell and at least one second Wallace tree cell, said at least one first Wallace tree cell structurally the same as said at least one second Wallace tree cell~~;

wherein said multiply-accumulate module includes a plurality of electrical paths which further include at least one critical path, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to a predetermined amount of time and less than a longest amount of time that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core, wherein said predetermined amount of time is less than said longest amount of time;

28   said plurality of Booth decoder cells includes at least one
29 first Booth decoder cell and at least one second Booth decoder
30 cell, said at least one first Booth decoder cell structurally the
31 same as said at least one second Booth decoder cells except that a
32 width of at least one of a first plurality of transistors of said
33 first Booth decoder cell is greater than a width of a corresponding
34 one of a second plurality of transistors of said second Booth
35 decoder cell;

36   said plurality of Wallace tree cells including at least one
37 first Wallace tree cell and at least one second Wallace tree cell,
38 said at least one first Wallace tree cell structurally the same as
39 said at least one second Wallace tree cell except that a width of
40 at least one of a first plurality of transistors of said first
41 Wallace tree cell is greater than a width of a corresponding one a
42 second plurality of transistors of said second Wallace tree cell;

43   wherein said at least one first Wallace tree cell ~~or~~ and said
44 at least one first Booth decoder cell are disposed on said at least
45 one critical path; and

46   wherein said at least one second Wallace tree cell and said at
47 least one second Booth decoder cell are disposed on an electrical
48 path not said at least one critical path and are not disposed on
49 any of said at least one critical path~~;~~

50 ~~wherein said at least one first Wallace tree cell or said at~~
51 ~~least one first Booth decoder cell comprises a first plurality of~~
52 ~~transistors, and at least one second Wallace tree cell or at least~~
53 ~~one second Booth decoder cell comprises a second plurality of~~
54 ~~transistors; and~~

55 ~~a width of at least one of said first plurality of transistors~~
56 ~~of said at least one first Wallace tree cell or said at least one~~
57 ~~first Booth decoder cell is greater than a width of a corresponding~~
58 ~~one of said second plurality of transistors of a corresponding one~~

59 ~~of said at least one second Wallace tree cell and said at least one~~
60 ~~second Booth decoder cell.~~

2.   (Canceled)

1   3.   (Previously Presented) The multiply-accumulate module of claim
2   1, wherein said multiply-accumulate core further comprises:
3   an adder connected to at least one of said Wallace tree cells;
4   a saturation detector connected to said adder, wherein said
5   multiply-accumulate module further comprises:
6   at least one input register connected to at least one of said
7   Booth encoding cells; and
8   at least one result register connected to said saturation
9   detector.

4 to 8.   (Canceled)

1   9.   (Original) The multiply-accumulate module of claim 1, wherein
2   said at least one second cell is a most significant bit or a least
3   significant bit and said at least one first cell is not a most
4   significant bit or a least significant bit.

1   10.   (Currently Amended) A parallel multiplier comprising:
2   a parallel multiplier core, wherein said parallel multiplier
3   core comprises:
4   a plurality of Booth encoder cells;
5   a plurality of Booth decoder cells connected to at least
6   one of said Booth encoder cells~~, said plurality of Booth decoder~~
7   ~~cells including at least one first Booth decoder cell and at least~~
8   ~~one second Booth decoder cell, said at least one first Booth~~
9   ~~decoder cell structurally the same as said at least one second~~
10 ~~Booth decoder cells~~; and

11   a plurality of Wallace tree cells connected to at least
12 one of said Booth decoder cells, ~~said plurality of Wallace tree~~
13 ~~cells including at least one first Wallace tree cell and at least~~
14 ~~one second Wallace tree cell, said at least one first Wallace tree~~
15 ~~cell structurally the same as said at least one second Wallace tree~~
16 ~~cell~~;

17   wherein said ~~multiply-accumulate module~~ <u>parallel</u> <u>multiplier</u>
18 includes <u>a</u> <u>plurality</u> <u>of</u> <u>electrical</u> <u>paths</u> <u>which</u> <u>further</u> <u>include</u> at
19 least one critical path, said at least one critical path being an
20 electrical path for which an amount of time that it takes for an
21 electrical signal to travel from an input of said ~~multiply-~~
22 ~~accumulate~~ <u>parallel</u> <u>multiplier</u> core to an output of said ~~multiply-~~
23 ~~accumulate~~ <u>parallel</u> <u>multiplier</u> core is greater than or equal to a
24 predetermined amount of time and less than a longest amount of time
25 that it takes any other electrical signal to travel from said input
26 of said ~~multiply accumulate~~ <u>parallel</u> <u>multiplier</u> core to said output
27 of said ~~multiply accumulate~~ <u>parallel</u> <u>multiplier</u> core, wherein said
28 predetermined amount of time is less than said longest amount of
29 time;

30   <u>said</u> <u>plurality</u> <u>of</u> <u>Booth</u> <u>decoder</u> <u>cells</u> <u>includes</u> <u>at</u> <u>least</u> <u>one</u>
31 <u>first</u> <u>Booth</u> <u>decoder</u> <u>cell</u> <u>and</u> <u>at</u> <u>least</u> <u>one</u> <u>second</u> <u>Booth</u> <u>decoder</u>
32 <u>cell,</u> <u>said</u> <u>at</u> <u>least</u> <u>one</u> <u>first</u> <u>Booth</u> <u>decoder</u> <u>cell</u> <u>structurally</u> <u>the</u>
33 <u>same</u> <u>as</u> <u>said</u> <u>at</u> <u>least</u> <u>one</u> <u>second</u> <u>Booth</u> <u>decoder</u> <u>cells</u> <u>except</u> <u>that</u> <u>a</u>
34 <u>width</u> <u>of</u> <u>at</u> <u>least</u> <u>one</u> <u>of</u> <u>a</u> <u>first</u> <u>plurality</u> <u>of</u> <u>transistors</u> <u>of</u> <u>said</u>
35 <u>first</u> <u>Booth</u> <u>decoder</u> <u>cell</u> <u>is</u> <u>greater</u> <u>than</u> <u>a</u> <u>width</u> <u>of</u> <u>a</u> <u>corresponding</u>
36 <u>one</u> <u>of</u> <u>a</u> <u>second</u> <u>plurality</u> <u>of</u> <u>transistors</u> <u>of</u> <u>said</u> <u>second</u> <u>Booth</u>
37 <u>decoder</u> <u>cell;</u>

38   <u>said</u> <u>plurality</u> <u>of</u> <u>Wallace</u> <u>tree</u> <u>cells</u> <u>including</u> <u>at</u> <u>least</u> <u>one</u>
39 <u>first</u> <u>Wallace</u> <u>tree</u> <u>cell</u> <u>and</u> <u>at</u> <u>least</u> <u>one</u> <u>second</u> <u>Wallace</u> <u>tree</u> <u>cell,</u>
40 <u>said</u> <u>at</u> <u>least</u> <u>one</u> <u>first</u> <u>Wallace</u> <u>tree</u> <u>cell</u> <u>structurally</u> <u>the</u> <u>same</u> <u>as</u>
41 <u>said</u> <u>at</u> <u>least</u> <u>one</u> <u>second</u> <u>Wallace</u> <u>tree</u> <u>cell</u> <u>except</u> <u>that</u> <u>a</u> <u>width</u> <u>of</u>
42 <u>at</u> <u>least</u> <u>one</u> <u>of</u> <u>a</u> <u>first</u> <u>plurality</u> <u>of</u> <u>transistors</u> <u>of</u> <u>said</u> <u>first</u>

43 Wallace tree cell is greater than a width of a corresponding one a
44 second plurality of transistors of said second Wallace tree cell;
45   wherein said at least one first Wallace tree cell ~~or~~ and said
46 at least one first Booth decoder cell are disposed on said at least
47 one critical path; and
48   wherein said at least one second Wallace tree cell and said at
49 least one second Booth decoder cell are disposed on an electrical
50 path not said at least one critical path and are not disposed on
51 any of said at least one critical path~~;~~
52   ~~wherein said at least one first Wallace tree cell or said at~~
53 ~~least one first Booth decoder cell comprises a first plurality of~~
54 ~~transistors, and at least one second Wallace tree cell or at least~~
55 ~~one second Booth decoder cell comprises a second plurality of~~
56 ~~transistors; and~~
57   ~~a width of at least one of said first plurality of transistors~~
58 ~~of said at least one first Wallace tree cell or said at least one~~
59 ~~first Booth decoder cell is greater than a width of a corresponding~~
60 ~~one of said second plurality of transistors of a corresponding one~~
61 ~~of said at least one second Wallace tree cell and said at least one~~
62 ~~second Booth decoder cell.~~

11. (Canceled)

1 12. (Previously Presented) The parallel multiplier of claim 10,
2 wherein said parallel multiplier core further comprises:
3   an adder connected to at least one of said Wallace tree cells;
4   a saturation detector connected to said adder, wherein said
5 parallel multiplier further comprises:
6   at least one input register connected to at least one of said
7 Booth encoding cells; and
8   at least one result register connected to said saturation
9 detector and at least one of said Wallace tree cells.

13 to 17. (Canceled)

18. (Currently Amended) The ~~multiply-accumulate~~ parallel multiplier of claim 10, wherein at least one second cell is a most significant bit or a least significant bit and at least one first cell is not a most significant bit or a least significant bit.

19. (Previously Presented) A method of designing a multiply-accumulate module comprising the steps of:
    providing a multiply-accumulate core, wherein the step of providing a multiply-accumulate core comprises the steps of:
        providing a plurality of Booth encoder cells;
        connecting a plurality of Booth decoder cells to at least one of said Booth encoder cells;
        connecting a plurality of Wallace tree cells to at least one of said Booth decoder cells;
        defining a predetermined amount of time greater than zero and less than a longest amount of time that it takes any electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core;
        defining at least one critical path within said multiply-accumulate module, said at least one critical path being an electrical path for which an amount of time that it takes for an electrical signal to travel from an input of said multiply-accumulate core to an output of said multiply-accumulate core is greater than or equal to ~~a~~ said predetermined amount of time and less than ~~a~~ said longest amount of time ~~that it takes any other electrical signal to travel from said input of said multiply-accumulate core to said output of said multiply-accumulate core, wherein said predetermined amount of time is less than said longest amount of time~~;

25   defining ~~a Wallace tree cell disposed on said at least~~

26 ~~one critical path as~~ a first Wallace tree cell <u>and a second Wallace</u>

27 <u>tree cell, said first Wallace tree cell structurally the same as</u>

28 <u>said second Wallace tree cell except that a width of at least one</u>

29 <u>of a first plurality of transistors of said first Wallace tree cell</u>

30 <u>is greater than a width of a corresponding one a second plurality</u>

31 <u>of transistors of said second Wallace tree cell;</u>

32   ~~defining a Wallace tree cell not disposed on any of said~~

33 ~~at least one critical path as second Wallace tree cell;~~

34   defining ~~a Booth decoder cell disposed on said at least~~

35 ~~one critical path as~~ a first Booth decoder cell <u>and a second Booth</u>

36 <u>decoder cell, said first Booth decoder cell structurally the same</u>

37 <u>as said second Booth decoder cell except that a width of at least</u>

38 <u>one of a first plurality of transistors of said first Booth decoder</u>

39 <u>cell is greater than a width of a corresponding one of a second</u>

40 <u>plurality of transistors of said second Booth decoder cell;</u>

41   ~~defining a Booth decoder cell not disposed on any of said~~

42 ~~at least one critical path as second Booth decoder cell;~~

43   ~~constructing each first Wallace tree cell and each first~~

44 ~~Booth decoder cell of a first plurality of transistors, each first~~

45 ~~Wallace tree cell structurally the same as each second Wallace tree~~

46 ~~cell, and constructing each second Wallace tree cell and each~~

47 ~~second Booth decoder cell of a second plurality of transistors,~~

48 ~~each first Booth decoder cell structurally the same as each second~~

49 ~~Booth decoder cell;~~

50   ~~selecting a first width for at least one of said first~~

51 ~~plurality of transistors of at least one of said first Wallace tree~~

52 ~~cell or said first Booth decoder cell; and~~

53   ~~selecting a second width for at least one of said second~~

54 ~~plurality of transistors of a second Wallace tree cell~~

55 ~~corresponding to said at least one of said first Wallace tree cell~~

56 ~~or of a second Booth decoder cell corresponding to said first Booth~~

57 ~~decoder cell which is less than said first width of a corresponding~~
58 ~~one of said first plurality of transistors~~
59 <u>disposing at least one first Wallace tree cell and at</u>
60 <u>least one first Booth decoder cell on said at least one critical</u>
61 <u>path;</u>
62 <u>disposing at least one second Wallace tree cell and said</u>
63 <u>at least one second Booth decoder cell are on an electrical path</u>
64 <u>not said at least one critical path; and</u>
65 <u>not disposing any second Wallace tree cell or any second</u>
66 <u>Booth decoder cell on any of said at least one critical path</u>.

1 20. (Currently Amended) A method of designing a parallel
2 multiplier comprising the steps of:
3 providing a parallel multiplier core, wherein the step of
4 providing a parallel multiplier core comprises the steps of:
5 providing a plurality of Booth encoder cells;
6 connecting a plurality of Booth decoder cells to at least
7 one of said Booth encoder cells;
8 connecting a plurality of Wallace tree cells to at least
9 one of said Booth decoder cells;
10 <u>defining a predetermined amount of time greater than zero</u>
11 <u>and less than a longest amount of time that it takes any electrical</u>
12 <u>signal to travel from said input of said parallel multiplier core</u>
13 <u>to said output of said parallel multiplier core;</u>
14 defining at least one critical path within said ~~multiply~~
15 ~~accumulate module~~ <u>parallel multiplier</u>, said at least one critical
16 path being an electrical path for which an amount of time that it
17 takes for an electrical signal to travel from an input of said
18 ~~multiply-accumulate~~ <u>parallel multiplier</u> core to an output of said
19 ~~multiply-accumulate~~ <u>parallel multiplier</u> core is greater than or
20 equal to ~~a~~ <u>said</u> predetermined amount of time and less than ~~a~~ <u>said</u>
21 longest amount of time ~~that it takes any other electrical signal to~~

22 travel from said input of said multiply accumulate core to said

23 output of said multiply accumulate core, wherein said predetermined

24 amount of time is less than said longest amount of time;

25   defining a Wallace tree cell disposed on said at least

26 one critical path as a first Wallace tree cell and a second Wallace

27 tree cell, said first Wallace tree cell structurally the same as

28 said second Wallace tree cell except that a width of at least one

29 of a first plurality of transistors of said first Wallace tree cell

30 is greater than a width of a corresponding one a second plurality

31 of transistors of said second Wallace tree cell;

32   defining a Wallace tree cell not disposed on any of said

33 at least one critical path as second Wallace tree cell;

34   defining a Booth decoder cell disposed on said at least

35 one critical path as a first Booth decoder cell and a second Booth

36 decoder cell, said first Booth decoder cell structurally the same

37 as said second Booth decoder cell except that a width of at least

38 one of a first plurality of transistors of said first Booth decoder

39 cell is greater than a width of a corresponding one of a second

40 plurality of transistors of said second Booth decoder cell;

41   defining a Booth decoder cell not disposed on any of said

42 at least one critical path as second Booth decoder cell;

43   constructing each first Wallace tree cell and each first

44 Booth decoder cell of a first plurality of transistors, each first

45 Wallace tree cell structurally the same as each second Wallace tree

46 cell, and constructing each second Wallace tree cell and each

47 second Booth decoder cell of a second plurality of transistors,

48 each first Booth decoder cell structurally the same as each second

49 Booth decoder cell;

50   selecting a first width for at least one of said first

51 plurality of transistors of at least one of said first Wallace tree

52 cell or said first Booth decoder cell; and

53 ~~selecting a second width for at least one of said second~~
54 ~~plurality of transistors of a second Wallace tree cell~~
55 ~~corresponding to said at least one of said first Wallace tree cell~~
56 ~~or of a second Booth decoder cell corresponding to said first Booth~~
57 ~~decoder cell which is less than said first width of a corresponding~~
58 ~~one of said first plurality of transistors~~
59 disposing at least one first Wallace tree cell and at
60 least one first Booth decoder cell on said at least one critical
61 path;
62 disposing at least one second Wallace tree cell and at
63 least one second Booth decoder cell are on an electrical path not
64 said at least one critical path; and
65 not disposing any second Wallace tree cell or any second
66 Booth decoder on any of said at least one critical path.